

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

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1 (Currently amended) An apparatus for detecting errors on a source-
2 synchronous bus, comprising:
3 the source-synchronous bus, wherein the source-synchronous bus includes
4 a plurality of data lines and a clock line;
5 a transmitting mechanism coupled to the source-synchronous bus, wherein
6 the transmitting mechanism is configured to transmit data on the source-
7 synchronous bus;
8 a receiving mechanism coupled to the source-synchronous bus, wherein
9 the receiving mechanism is configured to receive data from the source-
10 synchronous bus; and
11 an error detecting mechanism coupled to the receiving mechanism that is
12 configured to detect errors on the source-synchronous bus;
13 a grouping mechanism coupled to the transmitting mechanism that is
14 configured to group data bits into an error group, wherein the grouping
15 mechanism is further configured to skew data bits within the error group across
16 time;
17 a detection code generating mechanism coupled to the grouping
18 mechanism that is configured to generate a detection code for the error group; and
19 the transmitting mechanism that is further configured to transmit the
20 detection code on the source-synchronous bus using a clock cycle other than the
21 clock cycles used for transmitting data bits of the error group;

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22 | wherein data bits in the error group are transmitted at different times; and
23 | wherein the error detecting mechanism can detect errors on the plurality of
24 | data lines including errors that are caused by an error on the clock line.

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1 | 2. (Canceled).

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1 | 3. (Currently amended) The apparatus of claim 2claim 1, wherein the
2 | detection code is a parity bit.

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1 | 4. (Currently amended) The apparatus of claim 2claim 1, wherein the
2 | detection code is an error correcting code.

1 | 5. (Canceled).

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1 | 6. (Currently amended) The apparatus of claim 5claim 1, wherein skewing
2 | data bits across time includes delaying a data bit based on a position of the data bit
3 | within the error group.

1 | 7. (Currently amended) The apparatus of claim 5claim 1, further
2 | comprising a gathering mechanism coupled to the receiving mechanism, wherein
3 | the gathering mechanism is configured to de-skew data bits within the error group.

1 | 8. (Currently amended) A method for detecting errors on a source-
2 | synchronous bus, wherein the source-synchronous bus includes a plurality of data
3 | lines and a clock line, the method comprising:
4 | grouping data bits into an error group;
5 | skewing data bits within the error group across time;
6 | generating a detection code for the error group;

WIP

7 | transmitting data from a source on the source-synchronous bus;
8 | transmitting the detection code on the source-synchronous bus using a
9 | clock cycle other than the clock cycles used for transmitting data bits of the error
10 | group;
11 | receiving data at a destination from the source-synchronous bus; and
12 | detecting data errors at the destination, wherein detecting data errors
13 | includes detecting errors that are caused by errors on the clock line.

1 | 9. (Canceled).

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1 | 10. (Currently amended) The method of claim 9claim 8, wherein the
2 | detection code is a parity bit.

1 | 11. (Currently amended) The method of claim 9claim 8, wherein the
2 | detection code is an error correcting code.

1 | 12. (Canceled).

WIP

1 | 13. (Currently amended) The method of claim 12claim 8, wherein skewing
2 | data bits across time includes delaying a data bit based on a position of the data bit
3 | within the error group.

1 | 14. (Currently amended) The method of claim 12claim 8, further
2 | comprising de-skewing data bits within the error group.

1 | 15. (Currently amended) A computing system for detecting errors on a
2 | source-synchronous bus, comprising:

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3 the source-synchronous bus, wherein the source-synchronous bus includes
4 a plurality of data lines and a clock line;
5 a central processing unit coupled to the source-synchronous bus, wherein
6 the central processing unit is configured to transmit data on the source-
7 synchronous bus;
8 a memory unit coupled to the source-synchronous bus, wherein the
9 memory unit is configured to receive data from the source-synchronous bus;
10 an error detecting mechanism coupled to the memory unit that is
11 configured to detect errors on the source-synchronous bus;
12 a grouping mechanism coupled to the transmitting mechanism that is
13 configured to group data bits into an error group, wherein the grouping
14 mechanism is further configured to skew data bits within the error group across
15 time:
16 a detection code generating mechanism coupled to the grouping
17 mechanism that is configured to generate a detection code for the error group; and
18 the transmitting mechanism that is further configured to transmit the
19 detection code on the source-synchronous bus using a clock cycle other than the
20 clock cycles used for transmitting data bits of the error group;
21 wherein data bits in the error group are transmitted at different times; and
22 wherein the error detecting mechanism can detect errors on the plurality of
23 data lines including errors that are caused by an error on the clock line.

1 16. (Canceled).

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1 17. (Currently amended) The computing system of claim 16claim 15,
2 wherein the detection code is a parity bit.

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18. (Currently amended) The computing system of claim 16claim 15,
wherein the detection code is an error correcting code.

1 | 19. (Canceled).

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20. (Currently amended) The computing system of claim 19claim 15,
wherein skewing data bits across time includes delaying a data bit based on a
position of the data bit within the error group.

1 | 21. (Currently amended) The computing system of claim 19claim 15,
2 further comprising a gathering mechanism coupled to the memory unit, wherein
3 the gathering mechanism is configured to de-skew data bits within the error group.
